AF 2195

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:		
Kardach		
Serial No.: 09/606,839		Art Unit: 2195
Filed: June 28, 2000		Examiner:Banankhah, Majid A.
For: Method and Apparatus for Providing Real-Time Operation in a Personal Computer System		

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant (hereinafter "Appellant") hereby submit this Brief in support of its appeal from a final decision by the Examiner, mailed January 9, 2006, in the above-captioned case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences (hereinafter "Board") for allowance of the above-captioned patent application.

An oral hearing is not desired.

FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that I am causing the above-referenced correspondence to be deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and that this paper or fee has been addressed to Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: 6/7/06
Name of Person Mailing Correspondence: Leah Schwenke

Leah Schwenke
Signature

6/7/06
Date

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I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052, USA.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-20 are currently pending in the above-referenced application. No claims have been allowed. Claims 1-20 are the subject of this appeal.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action, mailed on January 9, 2006 (hereinafter "*Office Action*"), rejecting claims 1-20, Appellant timely filed a Notice of Appeal on April 7, 2006.

A copy of all claims on appeal is attached hereto as an Appendix of Claims.

V. SUMMARY OF THE INVENTION

According to one embodiment, a method is described. The method includes receiving real-time analog data at a personal computer implementing a general purpose operating system. Subsequently, a real-time interrupt indicating a request is generated to process the real-time data at a central processing unit (CPU). It is then determined whether the real-time interrupt has a higher priority than a non-real time operation already being processed at the CPU. If the real-time data has a higher priority, the CPU then processes the real-time data. See page 8, lines 19-23 – page 9, lines 1-11.

In a further embodiment, a computer system is described. The computer system includes a chipset, a bus, and a CPU. The chipset and CPU are coupled to the bus. The CPU generates a real-time interrupt upon receiving real-time analog data. If the real-time interrupt has a higher priority than a non-real-time operation currently being processed, the real-time data is processed. See page 8, lines 19-23 – page 9, lines 1-11.

In another embodiment, a central processing unit (CPU) is described. The CPU includes a timer, a register, an event mechanism and an event handler. The timer generates timing signals at predetermined time intervals. The register stores real-time data received at the CPU as analog data. The event mechanism is coupled to the timer and the register and generates real-time interrupts in response to receiving the timing signals. The event mechanism also determines if real-time data is stored within the register. The event handler is coupled to the event mechanism and upon determining the relative priority between the real-time interrupts and non-real-time operations being processed, the event handler processes data associated with the real-time interrupts received from the event mechanism. See page 8, lines 19-23 – page 9, lines 1-11.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-11, 13-15 and 19-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable MacDonald, U.S. Patent No. 6,295,574 (hereinafter "*MacDonald*"), in view of Simpson et al., EP 0742522 (hereinafter "*Simpson*"), and further in view of Maupin, U.S. Patent No. 6,154,832 (hereinafter "*Maupin*").

Claims 12 and 16-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *MacDonald*, in view of *Simpson* and *Maupin*, and further in view of Williams, U.S. Patent No. 5,764,582 (hereinafter "*Williams*").

VII. ARGUMENTS

1. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(a) BECAUSE ANY COMBINATION OF *MACDONALD*, *SIMPSON* AND *MAUPIN* DOES NOT DISCLOSE OR SUGGEST DETERMINING WHETHER A REAL-TIME INTERRUPT HAS A HIGHER PRIORITY THAN A NON-REAL TIME OPERATION BEING PROCESSED AT A CPU

Appellant respectfully submits that *MacDonald* in view of *Simpson* further in view of *Maupin* fails to disclose or suggest the claimed invention for the reasons set forth below. As the Honorable Board is well aware, in order to establish a *prima facie* case of obviousness:

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, *the prior art reference (or references when combined) must teach or suggest all the claim limitations*." (Emphasis added). *In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual of Patent Examining Procedure (MPEP), 8th Edition, Revision 2, May 2004, §2143.

(A) Claims 1-11, 13-15 and 19-20 were improperly rejected because *MacDonald* in view of *Simpson* further in view of *Maupin* does not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU

Claims 1-11, 13-15 and 19-20 are not obvious in view of *MacDonald* and *Simpson* further in view of *Maupin* under 35 U.S.C. § 103(a). For example, Appellant's claim 1 recites:

A method comprising:

receiving real-time analog data at a personal computer implementing a general purpose operating system;

generating a real-time interrupt indicating a request to process the real time data at a central processing unit (CPU);

determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at the CPU; and

processing the real-time data if the real-time interrupt has a higher priority than the non-real time operation.

Appellant's claim 7 recites:

A computer system comprising:

a chipset;

a bus coupled to the chipset; and

a central processing unit (CPU), coupled to the bus, to generate a real-time interrupt upon receiving real-time analog data and to process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed.

Appellant's claim 13 recites:

A central processing unit (CPU) comprising:

a timer to generate timing signals at predetermined time intervals;

a register to store real-time data received at the CPU as analog data;

an event mechanism coupled to the timer and the register to generate real-time interrupts in response to receiving the timing signals and determining that real-time data is stored within the register; and

an event handler coupled to the event mechanism to process data associated with the real-time interrupts received from the event mechanism upon determining the relative priority between the real-time interrupts and non-real-time operations being processed.

MacDonald discloses a CPU that includes a real time interrupt control unit configured to control real time capabilities of the CPU. See *MacDonald* at Abstract. *MacDonald* further discloses that instead of using interrupt acknowledge cycles normally used to locate an interrupt vector, an interrupt descriptor is stored in a real time interrupt

register which is coupled to the real time interrupt control unit. This causes the real time interrupt control unit to rapidly determine the fetch address of the real time interrupt. See *MacDonald* at col. 3, ll. 50-63.

However, *MacDonald* does not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU. The Examiner, in the Office Action, acknowledged that *MacDonald* fails to teach of a step or means for determining the real time interrupts among the interrupts (real time and non-real time). See Office Action at page 4, point 4. Instead, the Examiner cites *Simpson* as including such a feature.

Simpson discloses arbiter circuitry connected to storage circuitry for determining the priority status of each interrupt signal and selecting the one interrupt signal with the highest priority status. The arbiter circuitry then outputs an interrupt identifier associated with the selected interrupt signal. See *Simpson* at col. 1, ll. 46-56. Nonetheless, *Simpson* does not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU.

Maupin discloses a processor employing multiple register sets to eliminate interrupts. *Maupin* further discloses that one register is dedicated to interrupt sources, and another is dedicated to (non-interrupt) tasks. See *Maupin* at Abstract. *Maupin* discloses providing service routines for the processor for requests typically made by signaling interrupts. See *Maupin* at col. 2, ll. 24-26. The service routines are stored in the register dedicated to interrupt sources. The service routines are then executed by accessing the register. See *Maupin* at col. 2 ll. 65 – col. 3 ll. 4. Accordingly, the use of these service routines eliminates interrupt signals from the processor. See *Maupin* at col.

4, ll. 17-18. However, *Maupin* fails to disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU.

Appellant submits that *MacDonald*, *Simpson* and *Maupin* all fail to disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU.

Even though *Simpson* discloses a processor interrupt control system that determines the priority of interrupts, the interrupts are not real-time interrupts. Real-time interrupts are very time sensitive and therefore require much faster processing than do non real-time interrupts. A system designed to handle non real-time interrupts, as disclosed in *Simpson*, could not be used to handle the addition of real-time interrupts.

Since *MacDonald*, *Simpson* or *Maupin* do not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU, any combination of *MacDonald*, *Simpson* and *Maupin* would also not disclose or suggest the feature.

Further, Appellant submits that there is no motivation provided in any of the references themselves to combine *MacDonald*, *Simpson* and *Maupin*. As discussed above, the system in *MacDonald* is directed at handling real time interrupts in CPUs, *Simpson* relates to arbiter circuitry that is used to determine the priority level of various interrupts, and *Maupin* is a processor employing multiple sets of registers to eliminate interrupts. Appellant submits that it would not be obvious to combine the cited references since *Maupin* is eliminating interrupts, as opposed to generating them, while *MacDonald* and *Simpson* rely on the generation of interrupts. Because *Maupin* teaches

away from *MacDonald* and *Simpson*, the combining of *MacDonald, Simpson* and *Maupin* is not a proper combination under 35 U.S.C. §103(a).

Consequently, the Examiner has not established a prima facie case of obviousness, and the Examiner's rejection of claims 1-11, 13-15 and 19-20 under 35 U.S.C. §103(a) as being obvious over the combination of *MacDonald* in view of *Simpson* further in view of *Maupin* should be reversed.

Claims 2-6 and 17-18 depend from claim 1, claims 8-12 and 19-20 depend from claim 7, claims 14-16 depend from claim 13. Given that dependent claims necessarily include the limitations of the claims from which they depend, Appellant submits that the invention as claimed in claims 2-6, 8-12 and 14-20 are similarly patentable over *MacDonald* in view of *Simpson* further in view of *Maupin*.

Thus, the Examiner erred in rejecting claims 1-11, 13-15 and 19-20 under 35 U.S.C. § 103(a).

2. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(a) BECAUSE ANY COMBINATION OF *MACDONALD, SIMPSON, MAUPIN* AND *WILLIAMS* DOES NOT DISCLOSE OR SUGGEST DETERMINING WHETHER A REAL-TIME INTERRUPT HAS A HIGHER PRIORITY THAN A NON-REAL TIME OPERATION BEING PROCESSED AT A CPU

Appellant respectfully submits that *MacDonald, Simpson* and *Maupin* in view of *Williams* fail to disclose or suggest the claimed invention for the reasons set forth below.

(A) Claims 12 and 16-18 were improperly rejected because *MacDonald, Simpson* and *Maupin* in view of *Williams* does not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU

Claims 12 and 16-18 are not obvious in view of *MacDonald, Simpson* and *Maupin* in view of *Williams* under 35 U.S.C. §103(a).

As discussed above, nowhere do *MacDonald, Simpson* and *Maupin* disclose or suggest each and every element of the Appellant's independent claims. For example, *MacDonald, Simpson* and *Maupin* do not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU.

Williams discloses a bus that communicates data between a digital signal processor and a hardware interface, which includes digital-to-analog and analog-to-digital converters. See *Williams* at col. 4, ll. 26-28. Nevertheless, *Williams* does not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU. Since *MacDonald, Simpson* and *Maupin* fail to disclose all of the elements included in the Appellant's independent claim, including claim 1, and since *Williams* fails to disclose or suggest those elements missing from *MacDonald, Simpson* and *Maupin*, the combination of *MacDonald, Simpson, Maupin* and

Williams fails to disclose or suggest each and every element of the Appellant's invention as embodied in the claims. Consequently, the Examiner has not established a prima facie case of obviousness, and the Examiner's rejection of claims 12 and 16-18 under 35 U.S.C. §103(a) as being obvious over the combination of *MacDonald*, *Simpson*, *Maupin* and *Williams* should be reversed.

VIII. CONCLUSION

Appellant respectfully submits that all the appealed claims in this application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted with a check for $500.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overpayment to out Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: June 7, 2006

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IX. APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(9))

1. A method comprising:

receiving real-time analog data at a personal computer implementing a general purpose operating system;

generating a real-time interrupt indicating a request to process the real time data at a central processing unit (CPU);

determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at the CPU; and

processing the real-time data if the real-time interrupt has a higher priority than the non-real time operation.

2. The method of claim 1 further comprising continuing to process the non-real time operation if the real-time interrupt does not have a higher priority than the non- real time operation.

3. The method of claim 1 further comprising:

saving the state of the non-real time operation at the personal computer prior to processing the data associated with the real-time interrupt; and

processing the non-real time operation after processing of the data associated with the real-time interrupt has been completed.

4. The method of claim 1 further comprising:

receiving a non-real time interrupt while processing the real-time interrupt; and

determining whether the non-real time interrupt has a higher priority than the real-time interrupt.

5. The method of claim 4 further comprising:

continuing the processing of the real-time interrupt if the non-real time interrupt does not have a higher priority than the real time interrupt.

6. The method of claim 4 further comprising:

terminating the processing of the real-time interrupt if the non-real time interrupt has a higher priority; and

processing the non-real time interrupt.

7. A computer system comprising:

a chipset;

a bus coupled to the chipset; and

a central processing unit (CPU), coupled to the bus, to generate a real-time interrupt upon receiving real-time analog data and to process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed.

8. The computer system of claim 7 wherein the CPU comprises:

a timer to generate timing signals at predetermined time intervals; and

an event mechanism coupled to the timer to generate the real time interrupts.

9. The computer system of claim 8 wherein the CPU further comprises an event handler coupled to the event mechanism to process the real-time interrupts.

10. The computer system of claim 9 wherein the CPU further comprises a register coupled to the event mechanism to store real-time data.

11. The computer system of claim 9 wherein the event mechanism determines the relative priority between the real-time interrupts and the non-real-time operations.

12. The computer system of claim 11 wherein the CPU further comprises an analog to digital converter coupled to the register.

13. A central processing unit (CPU) comprising:

a timer to generate timing signals at predetermined time intervals;

a register to store real-time data received at the CPU as analog data;

an event mechanism coupled to the timer and the register to generate real-time interrupts in response to receiving the timing signals and determining that real-time data is stored within the register; and

an event handler coupled to the event mechanism to process data associated with the real-time interrupts received from the event mechanism upon determining the relative priority between the real-time interrupts and non-real-time operations being processed.

14. The CPU of claim 13 wherein the real-time analog data is data received from an analog radio coupled to the CPU.

15. The CPU of claim 13 wherein the event handler verifies whether there is data stored in register upon detecting a real-time interrupt and determines the priority of the real-time interrupt relative to other interrupts received.

16. The CPU of claim 13 wherein the CPU further comprises an analog to digital converter coupled to the register to convert the real-time analog data to digital data.

17. The method of claim 1 wherein receiving the real-time analog data comprises:

converting the real-time analog data to digital data; and

storing the digital data at a register.

18. The method of claim 17 wherein generating the real-time interrupt comprises:

receiving a timing signal at an event mechanism at a predetermined interval;

the event mechanism determining whether data is stored within the register; and

generating the real-time interrupt if data is stored within the register

19. The computer system of claim 10 wherein the event mechanism generates the real time interrupts in response to receiving the timing signals from the timer and determining that real-time data is stored within the register.

20. The computer system of claim 7 wherein the real-time analog data is data received from an analog radio.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDING APPENDIX

None.

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
Application Number	09/606,839
Filing Date	June 28, 2000
First Named Inventor	James P. Kardach
Examiner Name	Banankhah, Majid A
Art Unit	2195
Attorney Docket No.	42390P7017

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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☒ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
				Other fee (specify) _____	
				SUBTOTAL (2)	($) 500.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Mark L. Watson	Registration No. (Attorney/Agent)	46,322	Telephone	(303) 740-1980
Signature				Date	06/07/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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